

REMARKS

The Examiner's Office Action dated April 29, 2004 has been received and its contents reviewed. Accordingly, the above amendments have been made to independent claims 85, 91, 97, 103, 109 and 115. Support for the above amendments can be found at least at Figures 5A-5E, elements 506 (selected portion), 507 (first region, 508 (second region), and at page 23, line 20, to page 24, line 12). Therefore, claims 49-66 and 85-120 remain currently pending in the application with claims 85-120 being subject to examination; while claims 49-66 have been withdrawn from consideration as being directed to a non-elected invention. Reconsideration of the application in view of the above amendments and in light of the following remarks is respectfully requested.

Referring now to the detailed Office Action, the Applicants respectfully traverse each of the Examiner's rejections of:

Claims 85-87, 90-93, 96-99, 102-105, 108-111, 114-117 and 120, under 35 U.S.C. §102(b), as being anticipated by the teachings of Oka (JP '915), and

Claims 88, 89, 94, 95, 100, 101, 106, 107, 112, 113, 118 and 119, under 35 U.S.C. §103(a), as being obvious in view of the combination of teachings of Oka (JP '915) and the Kuznetsov (Inst. Phys. Conf.) article (taken with reference to Caune et al. article entitled "Combined CW Laser...With Some Metals", Applied Surface Sciences, (1989) Vol. 36, pages 597-604.

Each amended independent claim recites a method for manufacturing a semiconductor device including the steps of:

disposing a crystallizing promoting material in contact with a selected portion of the semiconductor film;

crystallizing the semiconductor film by heating wherein a crystal grows from said selected portion of the semiconductor film to a second portion of the semiconductor film adjacent to said selected portion;

patterning the crystallized semiconductor film to form an active layer wherein said active layer includes at least a first region and a second

region where said first region includes at least a part of the selected portion of the semiconductor film and said second region includes at least a part of the second portion of the semiconductor film;

...forming a wiring over the insulating film,

wherein the wiring is in contact with said first region of the active layer
(Emphasis added)

A review of the Oka reference, particularly the full English translation, and Figures 1(c), 1(d), 2(c), 2(d), 3(a), 3(b), 4 and 5, as well as the Examiner's comments at page 5, lines 7-12 of the final Office Action, reveals that the Examiner is mistaken in providing a broadest reasonable interpretation to the claimed phrase "selected portion" as including the "active region" of the independent claims. Specifically, the Examiner has misstated the requirements of the US case law which states that the claim limitations must be "given their broadest reasonable interpretation **consistent with the specification**" *In re Hyatt*, 211 F3f 1367; 54 USPQ2d 1664 (Fed. Cir. 2000) (emphasis added), see also MPEP Chapter 2111.

In the instant Detailed Description of the specification, at pages 23-25, this embodiment of the instant claims is clearly and succinctly set forth. In that section, the "selected portion" 506 of Figure 5A is set forth, as is the "active region" 515, 517, 518, 520 of Figure 5C. The "active region" is clearly stated to include two regions, a first region 506 and a second region 508 (arrow under masked areas showing lateral crystal growth), which are "the TFT region of the peripheral circuit...the former is composed of the crystalline silicon film..." see page 24, lines 7-12. Note, that in this embodiment the crystalline film is shown to be both the "selected portion" 506 and the lateral growth region shown by arrow 508. Further, the "wiring" 526, 527, 528 of Figure 5D is clearly shown to contact both the first and second regions of the "active region." In order to more clearly emphasize these teachings, each of the independent claims has been amended to essentially recite that the "...said active layer includes at least a first region and a second region where said first region includes at least a part

of the selected portion of the semiconductor film and said second region includes at least a part of the second portion of the semiconductor film;...forming a wiring over the insulating film, wherein the wiring is in contact with said first region of the active layer” (Emphasis added)

From this elaboration, it can be seen that the Examiner’s interpretation of the “selected portion” as being the active region of Oka is completely unreasonable and not consistent with the requirements of the case law or the guidance provided in MPEP Chapter 2111. For example, Oka does not teach, either implicitly or explicitly, **“wiring is in contact with said first region of the active layer.”** However, a detailed review of Oka reveals that the document does teach that the “selected portion” of Oka is in fact the “seed” region (FIG. 1(c), element 104; FIG. 2(c), element 204; FIG 3(b), element 203; FIG. 3(c), element 204; FIG. 4, element 403; FIG. 5, element 503) which in every embodiment Oka does not form any part of the active device region at all.

As highlighted in the Response of February 5, 2004, one of ordinary skill in the prior art, would understand from the translation of Oka that each process of forming TFT devices appreciates the patterning to remove the peripheral seed regions prior to forming the semiconductor islands which are to become the active device regions, and in each instance the wiring connections are made to the active portions of the remaining crystallized semiconductor island (second region of the present claims) which does not include the seed region. For these reasons, the Oka patent document does not teach each feature of the invention set forth in the independent claims 85, 91, 97, 103, 109 and 115, and, therefore, anticipation cannot exist.

Consequently, the rejection of claims 85-87, 90-93, 96-99, 102-105, 108-111, 114-117 and 120, under §102(b), over the teachings of Oka has been set forth in error and must now be withdrawn.

Turning to the Kuznetsov article (and the Caune et al. article cited in support

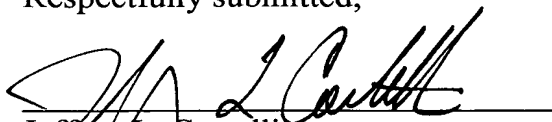
thereof), a review of that article reveals that Kuznetsov merely teaches specific concentrations for the crystallization promoting Ni formed in patterns on the a-Si substrate. Such a teaching does not in any manner cure the failure of Oka to teach forming the wiring connections to the seed (selected) portion of the active regions as presently claimed and certainly provides no motivation to one of ordinary skill in the prior art to modify the teachings of Oka so as not to remove the peripheral seed regions of Oka and instead utilize the seed regions as part of the active device regions, i.e., source/drain regions, to which the wiring connections are to be formed. For these reasons, a *prima facie* case of obviousness has not been established with regard to the teachings of Oka and the Kuznetsov article, and, consequently, the rejection of claims 88, 89, 94, 95, 100, 101, 106, 107, 112, 113, 118 and 119, under §103(a), has also been set forth in error and must now be withdrawn.

Finally, the Applicants again repeat the very specific request made in the Response of February 5, 2004, if the Examiner is to maintain, in the next office action, the position that Oka does in fact teach “forming an insulating film (FIG. 1(d), element 109) over the gate insulating film; and forming a wiring (FIG.1(d), element 111) over the insulating film, wherein the wiring is connected to the selected portion...,” then the Applicants specifically request that the Examiner provide a reasoned technical explanation (consistent with US case law and USPTO procedure) and supporting evidence (in Oka or other documentation) that Oka does in fact teach leaving the seed (selected) portion intact after crystallization and then teaches using the seed portion for the active regions of the semiconductor device, including forming wiring connections to the seed portions (i.e., the “selected portion” of the instant independent claims).

Thus, Applicants respectfully request consideration and allowance of the present application for the reasons provided above, i.e., it is submitted that claims 85-120 are now in condition for allowance. An early and favorable Notice of Allowance

is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Respectfully submitted,


Jeffrey L. Costellia
Registration No. 35,483

NIXON PEABODY LLP
401 9th Street, NW
Suite 900
Washington D.C. 20004
(202) 585-8000

JLC/JWM